KamLAND ATWD Testing Summary

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Abstract

This document describes the large scale ATWD testing for the KamLAND experiment. The testing procedure will be described and the results on the numbers of passed and failed chips will be given. Approximately 7750 chips were tested, with approximately 6120 passing the testing criteria.

1 Introduction

The Kamioka Liquid scintillator Anti-Neutrino Detector (KamLAND), currently under construction in Japan, is a long baseline neutrino oscillation experiment which uses Japanese commercial nuclear power reactors as the neutrino source. In the KamLAND reactor neutrino detector approximately 4000 Analog Transient Waveform Digitizer (AWTD) chips will be used to digitize the pulses from the 2000 17-inch photomultiplier tubes (two ATWD chips will be used for each PMT). Each of the ATWDs has four channels. In the KamLAND electronics, three of these will be used for PMT pulses (one high gain channel, one medium gain channel, and one low gain channel) and the fourth will be used for timing signals. We will refer to these channels as H, M, L, and X in this document. Each of the four channels has 128 bins. The time separation between bins can be tuned from 1 ns to 10 ns. Each bin stores a 10 bit digital number. A photograph of and ATWD chip is shown in Figure 1 and a sample waveform is shown in Figure 1.

2 Tester Setup

The testing board was fabricated from an existing 12-channel KamLAND prototype data acquisition board. The board was modified to power the ATWDs from an external source (to monitor the current consumption) and

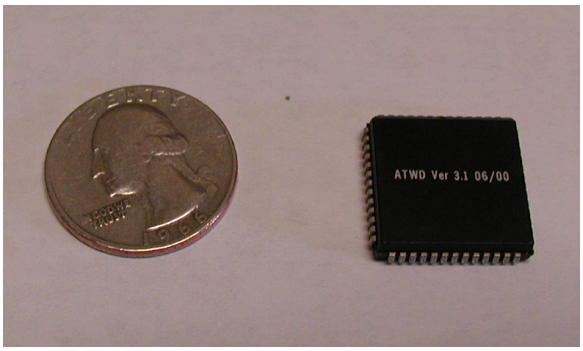

Figure 1: This photograph shows the ATWD sitting next to a quarter.

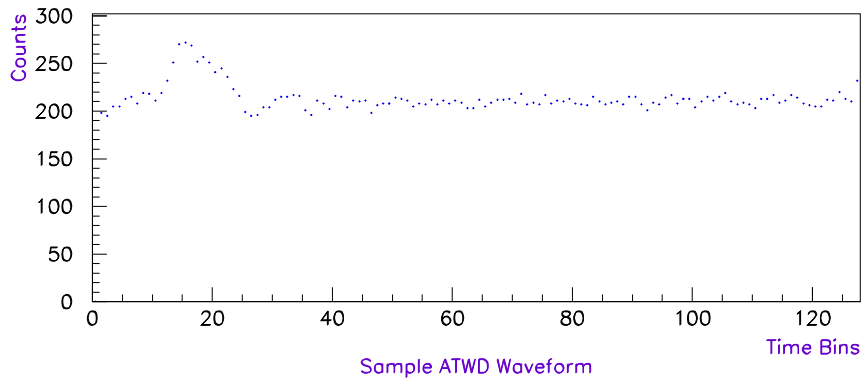

Figure 2: This photograph shows the ATWD output for a sample PMT pulse.

to include a computer-controlled pulser. The pulser could provide both very broad pulses (which would cover the entire ATWD digitization time) and high frequency pulses (approximately 20 MHz).

During the testing, the analog reference value used for the chips was 2.93 volts. The offset or pedestal voltage was approximately 2.61 volts. These voltage values were selected based on a sample of approximately 50 functional chips. If the pedestal gets too close to the analog reference voltage values, the chips cease to function properly and will shift out 0 counts. It was found that all chips are linear with these parameters down to approximately 740 mV. Below 740 mV, the chips become non-linear and will tend to output 1023 counts. In this initial testing phase on approximately 50 chips, the gain variations between the chips were also studied. The gain variations were found to be roughly 2%.

3 Testing Criteria and Procedure

The testing software was written by Sanshiro Enomoto using the Kinoko package. For the mass testing it was desired to study the power consumption, pedestal shape, linearity, gain, time response, and cross talk between channel for all of the ATWDs. These tests were applied to all four channels. In the testing program, data is collected and the chips must pass the 10 criteria given below. Note that these tests were applied in the order given here.

1: Bad Current The tester would first enter the current draw of the chip which appears on the power supply. If the current was less than 20 mA or greater than 30 mA the chip was rejected.

2: Does not Digitize If the chip did not respond within 1 second, it was rejected.

3: Bad Deviation Across Waveform during Pedestal Test For the pedestal check, no pulser signals were applied to the chip. Approximately 50 pedestal waveforms were obtained. The mean and deviation across the entire waveform was obtained. It the deviation was greater than 7 counts, the chip was rejected. The helped to catch chips with stuck bits. It was noted that the last three bins normally tended to have high pedestals and they were not included here. The pedestals were normally approximately 120 counts. The high gain channel (which was the first one read out) normally had a slightly lower pedestal than the other channels.

4: Bad Deviation in a Bin During Pedestal Test The same 50 waveforms discussed above were also analyzed to find the mean and deviation

on each of the 128 bins. If the deviation on any one bin was greater than 2 counts, the chip was rejected.

5: Samples Reach 0 or 1023 Throughout the pedestal and linearity tests, if any waveform had 3 or more bins with 0 or 1023 counts this chip was rejected. This was usually a sign of non-linearity.

6: Bad Linearity Slope For the linearity test, pulses of height 0 V, .48 V, .72 V, .96 V, 1.2 V, 1.44 V, 1.675 V. , and 1.87 V were applied to the chips. (These pulses were negative going and were added to the pedestal value of 2.61 V, i.e. the 0.48 V pulse had a max value of 2.61 and went down to 2.13 V.) These pulses were very broad and covered the entire ATWD acquisition time. The mean and deviation of these pulses was taken across the 128 bins. Since the chips generally tended to be linear in the middle of the voltage range, the mean values of the five middle pulses (.48 V to 1.675 V) were fit to a line. To provide some test of the chip gain, any chip with a slope (measured in counts per volt) less than 345 or greater than 430 was rejected.

7: Bad RMS across waveform during linearity test As mentioned above, the deviation for each of the 7 pulses in the linearity test was taken. If the deviation was large, it might indicate a stuck bit or non-linearity (the waves tended to become very jumpy as a chip was beginning to behave non-linearly). Any chip with a deviation greater than 10 counts was rejected.

8: Bad Linearity Extrapolation As mentioned above, only the five middle pulses were fit to a line. This line was then extrapolated to 0 V and 1.87 V. If either of the measured values for these voltages deviated from the extrapolation by more than 10 counts, the chip was rejected as it most likely was becoming non-linear.

9: Bad timing Chi Squared or Gain For the timing check, a high frequency (20 MHz) pulse was fed to the chip. The edges of these pulses were then found and the edge number was plotted as a function of the time bin location for that edge. For a uniform timing response, we would expect a straight line for this plot. The data were fit to a straight line. If the Chi squared of this fit was greater than .5, the chip was rejected. Also, to insure that the chips all had similar timing gains, if the slope of the line was greater than 18 or less than 15.5, the chip was rejected.

10: High Crosstalk One last concern was cross talk between the four channels. For this measurement, a 20 MHz pulse was applied to only one of the channels. The waves collected on the other three channels were then compared to the pedestals taken earlier in the testing process. If any bin changed by more than 30 counts, the chip was rejected. This was repeated for all four channels. Note that most of the cross talk came from the large chip socket and long wires used for the test board rather than from the chip.

Table 1: The table below shows the number of chips for each of the 10 failure modes. Recall that the failure mode shown here is only the first criteria which the chip failed on. This table contains 143 failed chips from the June 2000 chip batch and 1627 failed chips from the April 2001 batch.

Failure Mode	Number Failed
1	455
2	119
3	606
4	252
5	103
6	65
7	124
8	29
9	14
10	3
Total	1770

If a chip passes all of the above criteria, it was considered to be acceptable. If a chip failed one of the 10 criteria, it was rejected and the number of the first test it failed appeared on the screen so that chips with common failure modes could be separated.

For a detailed description of the testing procedure and how to use the testing software, please consult the ATWD testing procedure document.

4 Testing Results

Two different batches of silicon were tested, one from June 2000 and one from April 2001. The June batch contained 724 chips which were tested with 581 of these chips passing on the tester. The April 2001 batch had 7744 chips tested, with 6117 passing the test criteria. It was noted that the two batches has slightly different linearity and timing gains. Therefore, only chips from the April 2001 will be used in the KamLAND electronics.

Recall also that the failed chips were classified by which of the 10 criteria they failed on. The result are shown in the Table 1.

These results show that the total fraction of chips which passed the testing criteria was 80.2 % for the June 2000 batch and 79.0 % for the April 2001 batch. The most common failure modes were a bad RMS across the

128 channels for the pedestals and a bad current value. All of the failed chips have been stored according to their failure mode. Therefore if at some later date it was decided to relax some of the test criteria, it will be possible to retest the chips which failed that particular test.

References

[1] Marino, A. D., "Testing Procedure for the Analog Transient Waveform Digitizers", May 2001